

What is claimed is:

1 1. A method of forming a bit line contact via,
2 comprising:

3 providing a substrate with a transistor thereon, the
4 transistor having a gate electrode, drain region,
5 and source region;

6 forming a conductive layer overlying the drain region;
7 conformally forming an insulating barrier layer
8 overlying the substrate;

9 blanketly forming a dielectric layer overlying the
10 insulating barrier layer; and

11 forming a via through the dielectric layer and
12 insulating barrier layer, exposing the conductive
13 layer.

1 2. The method as claimed in claim 1, wherein forming
2 the conductive layer further comprises:

3 blanketly forming the conductive layer overlying the
4 substrate;

5 removing the unwanted conductive layer, leaving a
6 conductive layer thinner than the gate electrode,
7 overlying the drain region and source region;

8 forming a patterned resist layer exposing the
9 conductive layer overlying the source region;

10 removing the exposed conductive layer using the
11 patterned resist layer as a mask; and

12 removing the patterned resist layer.

1 3. The method as claimed in claim 1, wherein forming
2 the conductive layer further comprises:

3 conformally forming a metal/metal compound layer
4 overlying the substrate;

5 blanketly forming the conductive layer overlying the
6 substrate;

7 removing the unwanted conductive layer, remaining the
8 conductive layer, thinner than the gate
9 electrode, overlying the drain region and source
10 region;

11 forming a patterned resist layer exposing the
12 conductive layer overlying the source region;

13 removing the exposed conductive layer using the
14 patterned resist layer as a mask and the
15 metal/metal compound layer as a stop layer,
16 thereby exposing the metal/metal compound layer
17 overlying the source region; and

18 removing the patterned resist layer and exposed
19 metal/metal compound layer.

1 4. The method as claimed in claim 1, wherein forming
2 the conductive layer further comprises:

3 conformally forming a Ti/TiSi layer overlying the
4 substrate;

5 blanketly forming the conductive layer overlying the
6 substrate;

7 removing the unwanted conductive layer, leaving the
8 conductive layer thinner than the gate electrode,
9 overlying the drain region and source region;

10 forming a patterned resist layer exposing the
11 conductive layer overlying the source region;
12 removing the exposed conductive layer using the
13 patterned resist layer as a mask and the Ti/TiSi
14 layer as a stop layer, thereby exposing the
15 Ti/TiSi layer overlying the source region;
16 ashing the patterned resist layer using oxygen plasma;
17 and
18 removing the exposed metal/metal compound layer using
19 SPM (sulfuric acid-hydrogen peroxide mixture) and
20 APM (ammonium hydrogen peroxide mixture).

1 5. The method as claimed in claim 1, wherein the
2 conductive layer is doped polycrystalline silicon.

1 6. The method as claimed in claim 1, wherein the
2 insulating barrier layer is SiN.

1 7. The method as claimed in claim 1, wherein the
2 dielectric layer comprises an oxide.

1 8. The method as claimed in claim 1, wherein the
2 dielectric layer comprises boro-phosphosilicate glass
3 (BPSG).

1 9. The method as claimed in claim 3, wherein the
2 metal/metal compound layer comprises a Ti/TiSi layer.

1 10. The method as claimed in claim 5, wherein the
2 conductive layer is doped with an element in either group 13
3 (IIIA) or 15 (VA) of periodic table.

1 11. The method as claimed in claim 5, wherein the
2 conductive layer is doped with As.

1 12. A method of a forming bit line contact via,
2 comprising:

3 providing a substrate with a transistor thereon, the
4 transistor having a gate electrode, drain region,
5 and source region;

6 conformally forming a conductive layer overlying the
7 substrate;

8 blanketly forming a doped polycrystalline silicon layer
9 overlying the substrate;

10 removing the unwanted conductive layer and doped
11 polycrystalline silicon layer, leaving the doped
12 polycrystalline layer thinner than the gate
13 electrode, overlying the drain region, and the
14 conductive layer covered by the doped
15 polycrystalline silicon layer;

16 conformally forming an insulating barrier layer
17 overlying the substrate;

18 blanketly forming a dielectric layer overlying the
19 insulating barrier layer; and

20 forming a via through the dielectric layer and
21 insulating barrier layer, exposing the doped
22 polycrystalline silicon layer.

1 13. The method as claimed in claim 12, wherein removing
2 the unwanted conductive layer and doped polycrystalline
3 silicon layer further comprises:

4 removing a part of the doped polycrystalline silicon
5 layer using etching or chemical mechanical
6 polishing (CMP), thereby leaving the doped
7 polycrystalline silicon layer, thinner than the
8 gate electrode, overlying the drain region and
9 source region;

10 forming a patterned resist layer exposing the doped
11 polycrystalline silicon layer overlying the
12 source region;

13 removing the exposed polycrystalline silicon layer
14 using the patterned resist layer as a mask and
15 the conductive layer as a stop layer, thereby
16 exposing the conductive layer overlying the
17 source region; and

18 removing the patterned resist layer and exposed
19 conductive layer.

1 14. The method as claimed in claim 12, wherein the
2 conductive layer comprises a Ti/TiSi layer, and removing the
3 unwanted conductive layer and doped polycrystalline silicon
4 layer further comprises:

5 removing a part of the doped polycrystalline silicon
6 layer using etching or chemical mechanical
7 polishing (CMP), thereby leaving the doped
8 polycrystalline silicon layer thinner than the
9 gate electrode, overlying the drain region and
10 source region;

11 forming a patterned resist layer exposing the doped
12 polycrystalline silicon layer overlying the
13 source region;

14 removing the exposed polycrystalline silicon layer
15 using the patterned resist layer as a mask and
16 the conductive layer as a stop layer, thereby
17 exposing the conductive layer overlying the
18 source region;
19 ashing the patterned resist layer using oxygen plasma;
20 and
21 removing the exposed conductive layer using SPM
22 (sulfuric acid-hydrogen peroxide mixture) and APM
23 (ammonium hydrogen peroxide mixture).

1 15. The method as claimed in claim 12, wherein the
2 insulating barrier layer is SiN.

1 16. The method as claimed in claim 12, wherein the
2 dielectric layer comprises an oxide.

1 17. The method as claimed in claim 12, wherein the
2 dielectric layer comprises boro-phosphosilicate glass
3 (BPSG).

1 18. The method as claimed in claim 11, wherein the
2 doped polycrystalline silicon layer is doped with an element
3 in either group 13 (IIIA) or 15 (VA) of periodic table.

1 19. The method as claimed in claim 11, wherein the
2 doped polycrystalline silicon layer is doped with As.

1 20. A method of a forming bit line contact via,
2 comprising:

3 providing a substrate with a transistor thereon, the
4 transistor having a gate electrode, drain region,
5 and source region;
6 conformally forming a Ti/TiSi layer overlying the
7 substrate;
8 blanketly forming a doped polycrystalline silicon layer
9 overlying the substrate;
10 removing a part of the doped polycrystalline silicon
11 layer, leaving the doped polycrystalline silicon
12 layer thinner than the gate electrode, overlying
13 the drain region and source region;
14 forming a patterned resist layer exposing the doped
15 polycrystalline silicon layer overlying the
16 source region;
17 removing the exposed polycrystalline silicon layer
18 using the patterned resist layer as a mask and
19 the Ti/TiSi layer as a stop layer, thereby
20 exposing the Ti/TiSi layer overlying the source
21 region;
22 ashing the patterned resist layer using oxygen plasma;
23 removing the exposed Ti/TiSi layer using SPM (sulfuric
24 acid-hydrogen peroxide mixture) and APM (ammonium
25 hydrogen peroxide mixture);
26 conformally forming an SiN layer overlying the
27 substrate;
28 blanketly forming a dielectric layer overlying the SiN
29 layer; and
30 forming a via through the dielectric layer and SiN
31 layer, exposing the doped polycrystalline silicon
32 layer.